



223

PATENT  
Attorney Docket No. CDS-006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS: Bellantoni et al.  
SERIAL NO.: 10/820,435 GROUP NO.: 2123  
FILING DATE: 08-Apr-04 EXAMINER: Not yet assigned  
TITLE: *System-Level Simulation of Devices Having Diverse Timing*

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with the provisions of 37 C.F.R. 1.97 and 1.98, Applicants hereby make of record the patents and publications listed on the accompanying Form PTO-1449, and other information contained herein, for consideration by the Examiner in connection with the examination of the above-identified patent application. Copies of the patents and publications are enclosed.

REMARKS

In accordance with the provisions of 37 C.F.R. 1.97, this statement is being filed (CHECK ONE):

- ☒ (1) within three (3) months of the **filing date** of a national application other than a continued prosecution application under 37 C.F.R. 1.53(d), or within three (3) months of the **date of entry of the national stage** as set forth in 37 C.F.R. 1.491 in an international application, or before the mailing of the **first Office action** on the merits, or before the mailing of a **first Office action** after the filing of a request for continued examination under 37 C.F.R. 1.114; or
- ☐ (2) after the period defined in (1) but before the mailing date of a **final action** or a **notice of allowance** under 37 C.F.R. 1.311, and
- ☐ the requisite Statement is below, **OR**
- ☐ the requisite fee under 37 C.F.R. 1.17(p), namely **\$180.00**, is included herein, or
- ☐ (3) after the mailing date of a **final action** or **notice of allowance** but before the payment of the **issue fee**, **AND**

- ☐ the requisite Statement is below, **AND**
- ☐ the requisite petition fee under 37 C.F.R. 1.17(p), namely **\$180.00** is included herein.

It is respectfully requested that each of the patents and publications listed on the attached Form PTO-1449, and other information contained herein, be made of record in this application.

#### STATEMENT

As required under 37 C.F.R. 1.97(e), Applicant(s), through the undersigned, hereby state either that [check the appropriate space only if either (2) or (3) is checked on the previous page and the Statement is required]:

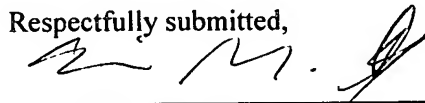
- ☐ 1. Each item of information contained in the Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application **not more than three months** prior to the filing of the Information Disclosure Statement; or
- ☐ 2. No item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing this Statement after making reasonable inquiry, no item of information contained in the Information Disclosure Statement was known to **any individual** designated in 37 C.F.R. 1.56(c) **more than three months** prior to the filing of the Information Disclosure Statement.

Date: January 26, 2005  
Reg. No. 44,691

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**CERTIFICATE OF FIRST CLASS MAILING UNDER 37 C.F.R. 1.8**

I hereby certify that this correspondence, and any document(s) referred to as enclosed herein, is/are being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 26<sup>th</sup> January 2005.

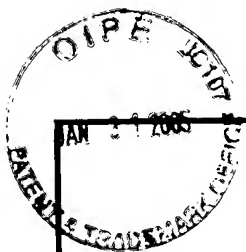
  
Monika A. Pychynska

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Submitted herewith is/are:

- (1) Transmittal Form (1 pg.);
- (2) Information Disclosure Statement (2 pgs.);
- (3) Form PTO-1449 (5 pg.); copies of references cited C1-C50;
- (4) and a return receipt postcard.



# TRANSMITTAL FORM

Application Serial Number	10'820.435
Filing Date	08-Apr-04
First Named Inventor	Bellantoni
Group Art Unit	2123
Examiner Name	Not yet assigned
Attorney Docket No.	CDS-006
Patent No.	Not applicable
Issue Date	Not applicable

## ENCLOSURES (check all that apply)

<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Check Attached <input type="checkbox"/> Copy of Fee Transmittal Form	<input type="checkbox"/> Copy of Notice to File Missing Parts of Application <input type="checkbox"/> Formal Drawing(s)	<input type="checkbox"/> Notice of Appeal to Board of Patent Appeals and Interferences <input type="checkbox"/> Appeal Brief (in triplicate)
<input type="checkbox"/> Amendment/Response <input type="checkbox"/> Preliminary <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Letter to Official Draftsperson including Drawings [Total Sheets _____]	<input type="checkbox"/> Request For Continued Examination (RCE) Transmittal <input type="checkbox"/> Power of Attorney (Revocation of Prior Powers) <input type="checkbox"/> Terminal Disclaimer	<input type="checkbox"/> Status Inquiry <input checked="" type="checkbox"/> Return Receipt Postcard <input checked="" type="checkbox"/> Certificate of First Class Mailing under 37 C.F.R. 1.8 <input type="checkbox"/> Certificate of Facsimile Transmission under 37 C.F.R. 1.8
<input type="checkbox"/> Petition for Extension of Time	<input type="checkbox"/> Executed Declaration and Power of Attorney for Utility or Design Patent Application	<input type="checkbox"/> Additional Enclosure(s) (please identify below)
<input checked="" type="checkbox"/> Information Disclosure Statement <input checked="" type="checkbox"/> Form PTO-1449 <input checked="" type="checkbox"/> Copies of IDS Citations C1-C50	<input type="checkbox"/> Small Entity Statement <input type="checkbox"/> CD(s) for large table or computer program	
<input type="checkbox"/> Certified Copy of Priority Document(s)	<input type="checkbox"/> Amendment After Allowance	
<input type="checkbox"/> Sequence Listing submission <input type="checkbox"/> Paper Copy/CD <input type="checkbox"/> Computer Readable Copy <input type="checkbox"/> Statement verifying identity of above	<input type="checkbox"/> Request for Certificate of Correction <input type="checkbox"/> Certificate of Correction (in duplicate)	

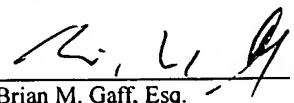
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FORM PTO - 1449				ATTORNEY DOCKET NO.: CDS-006			
INFORMATION DISCLOSURE STATEMENT				APPLICANTS: Bellantoni et al.			
				SERIAL NO.: 10/820,435			
				FILING DATE: 8-Apr-2004 GROUP: 2123			
U.S. PATENT DOCUMENTS							
EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A1	5,062,067	29-Oct-91	Schaefer et al.	364	578	15-Mar-89
	A2	5,437,037	25-Jul-95	Furuichi	395	700	7-Jun-93
	A3	5,502,661	26-Mar-96	Glunz	364	578	7-Oct-93
	A4	5,544,067	6-Aug-96	Rostoker et al.	364	489	14-Jun-93
	A5	5,696,942	9-Dec-97	Palnitkar et al.	395	500	24-Mar-95
	A6	5,768,567	16-Jun-98	Klein et al.	395	500	14-May-96
	A7	5,784,593	21-Jul-98	Tseng et al.	395	500	29-Sep-95
	A8	5,809,283	15-Sep-98	Vaidyanathan et al.	395	500	29-Sep-95
	A9	5,862,361	19-Jan-99	Jain	395	500	7-Sep-95
	A10	5,880,975	9-Mar-99	Mangelsdorf	364	578	5-Dec-96
	A11	5,978,571	2-Nov-99	Grundmann	395	500	12-May-97
	A12	5,991,523	23-Nov-99	Williams et al.	395	500.19	18-Mar-97
	A13	6,052,524	18-Apr-00	Pauna	395	500.43	14-May-98
	A14	6,134,516	17-Oct-00	Wang et al.	703	27	5-Feb-98
	A15	6,135,647	24-Oct-00	Balakrishnan et al.	395	500.19	23-Oct-97
	A16	6,152,612	28-Nov-00	Liao et al.	395	500	9-Jun-97
	A17	6,175,946 B1	16-Jan-01	Ly et al.	716	4	20-Oct-97
	A18	6,182,258 B1	30-Jan-01	Hollander	714	739	6-Feb-98
	A19	6,223,144 B1	24-Apr-01	Barnett et al.	703	22	24-Mar-98
	A20	6,295,517 B1	25-Sep-01	Roy et al.	703	15	7-Apr-98
	A21	6,321,363 B1	20-Nov-01	Huang et al.	716	4	11-Jan-99
	A22	6,466,898 B1	15-Oct-02	Chan	703	17	12-Jan-99
EXAMINER				DATE CONSIDERED			

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<b>FOREIGN PATENT DOCUMENTS</b>									
<b>EXAM. INIT.</b>		<b>DOCUMENT NUMBER</b>	<b>DATE</b>	<b>COUNTRY CODE</b>	<b>CLASS</b>	<b>SUB CLASS</b>	<b>FILING DATE</b>	<b>ABSTRACT ONLY</b>	<b>ENGLISH LANG (Y/N)</b>
<b>OTHER ART, JOURNAL ARTICLES, ETC.</b>									
<b>EXAM. INIT.</b>	<b>OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)</b>								
	C1	Andrews, J., Axis Systemss Inc., "Co-verification speeds SOC design," EDN, September 5, 2002, pp. 95-96, 98, 100.							
	C2	Axis Systems, Inc, "Xpert™ ARM® Solution," Datasheet, <a href="http://www.AxisSystems.com">www.AxisSystems.com</a> , 2 pages.							
	C3	Becker, M., "Faster Verilog Simulations Using a Cycle Based Programming Methodology," <i>Proceedings 1996 IEEE International Verilog HDL Conference</i> , Feb. 26-28, 1996, Santa Clara, CA, USA: IEEE Computer Society Press, 1996, pp. 24-31.							
	C4	Bell, G., "Solidification – Static Functional Verification with Solidify," HDAC, Inc., 8 pages.							
	C5	Björklund, D. et al., "A Language for Multiple Models of Computation," <i>Proceedings of the Tenth International Symposium on Hardware/Software Codesign</i> , May 6-8, 2002, Estes Park, CO, USA: CODES 2002, 2002 ACM, pp. 25-30.							
	C6	Braun, G. et al., "Using Static Scheduling Techniques for the Retargeting of High Speed, Compiled Simulators for Embedded Processors from an Abstract Machine Description," <i>International Symposium on System Synthesis</i> , Sept. 30-Oct. 3, 2001, Montreal, Quebec, Canada: 2001 ACM, pp. 57-62.							
	C7	Chatelain, A. et al., "High-Level Architectural Co-Simulation Using Esterel and C," <i>Proceedings of the Ninth International Workshop on Hardware/Software Codesign/CASHE</i> , April 25-27, 2001, Copenhagen, Denmark: 2001 ACM, pp. 189-194.							
	C8	Choi, K. et al., "Incremental-in-time algorithm for digital simulation" <i>Proceedings of the Design Automation Conference</i> . Anaheim, June 12-15, 1988, <i>Proceedings of the Design Automation Conference</i> . Anaheim (DAC), New York, IEEE, US, vol. CONF. 25, 12-Jun-1988, pages 501-505.							
	C9	Clarke, P., "Cambridge startup claims speedier simulation tools," <i>EE Times</i> , <a href="http://www.eetimes.com/story/OEG2000424S0041">http://www.eetimes.com/story/OEG2000424S0041</a> ; April 24, 2000, 2 pages.							
<b>EXAMINER</b>					<b>DATE CONSIDERED</b>				

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OTHER ART, JOURNAL ARTICLES, ETC.		
C10	Clarke, P., "EDA tool generates bit- and cycle-accurate C code," <i>EE Times</i> , <a href="http://www.eetimes.com/story/OEG20010713S0069">http://www.eetimes.com/story/OEG20010713S0069</a> ; July 13, 2001, 1 page.	
C11	Clarke, P., "Tenison tool draws Verilog into SystemC compilation," <i>EEdesign</i> , <a href="http://www.eedesign.com/article/showArticle.jhtml?articleID=17406761">http://www.eedesign.com/article/showArticle.jhtml?articleID=17406761</a> ; December 18, 2000, 2 pages.	
C12	Creusillet, B. et al., "Interprocedural analyses of Fortran programs" <i>Parallel Computing</i> , Elsevier Publishers, Amsterdam, NL, vol. 24, no. 3-4, May 1998, pages 629-648.	
C13	DeVane, C. J., "Efficient circuit partitioning to extend cycle simulation beyond synchronous circuits" <i>Computer-Aided Design</i> , 1997. Digest of Technical Papers., 1997 IEEE/ACM International Conference on San Jose, CA, USA 9-13 Nov. 1997.	
C14	Donnelly, K., "High performance VHDL simulation using native compiled code" <i>Electronic Engineering</i> , Morgan-Grampian LTD. London, GB, vol. 65, no. 803, 01-Nov.1993, page 51, 53, 55, 57.	
C15	Duarte, D. et al., "Evaluating the Impact of Architectural-Level Optimizations on Clock Power," <i>Proceedings of the 14<sup>th</sup> Annual IEEE International ASIC/SOC Conference</i> , Sept. 12-15, 2001, Arlington, VA, USA: 2001 IEEE, pp. 447-451.	
C16	Edwards, C., "Two startups jump into co-verification," <i>EEdesign</i> , <a href="http://www.design.com/article/printableArticle.jhtml?articleID=17407943">http://www.design.com/article/printableArticle.jhtml?articleID=17407943</a> ; September 23, 2002, 3 pages.	
C17	Edwards, C., "U.K.'s Celoxica, Tenison enter-co-verification fray," <i>Electronic Engineering Times</i> , October 14, 2002, pp. 24, 27.	
C18	Edwards, S. A., "Compiling Esterel into sequential code" <i>Proc Des Autom Conf; Proceedings - Design Automation Conference 2000 IEEE</i> , Piscataway, NJ, USA, 2000, pages 322-327.	
C19	French, R.S. et al., "A General Method for Compiling Event-Driven Simulations," Stanford University, <a href="http://suif.stanford.edu/papers/rfrench95/paper.html">http://suif.stanford.edu/papers/rfrench95/paper.html</a> ; 19 pages.	
C20	Greaves, D., Tenison Technology, "VTOC Verilog -> C," <i>International Workshop on Rapid System Prototyping</i> , Tenison TechEDA, <a href="http://www.tenisontech.com">www.tenisontech.com</a> , pp. 1-12.	
C21	Gupta, S. et al., "Conditional Speculation and its Effects on Performance and Area for High-Level Synthesis," <i>International Symposium on System Synthesis</i> , Sept. 30-Oct. 3, 2001, Montreal, Quebec, Canada: 2001 ACM, pp. 171-176.	
C22	Hoffman, A. et al., "A Framework for Fast Hardware-Software Co-simulation," <i>Proceedings; Design, Automation and Test in Europe. Conference and Exhibition 2001</i> , Munich, Germany, March 13-16, 2001. IEEE Computer Society 2001, pp. 760-764.	
C23	International Search Report PCT/US 03/35649 dated 01-Dec-04	
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C24	International Search Report PCT/US 03/35403 dated 14-Dec-04	
C25	International Search Report PCT/US 03/35508 dated 05-Jan-05	
C26	Iyer, A. et al., "Power and Performance Evaluation of Globally Asynchronous Locally Synchronous Processors," <i>Proceedings of the 29<sup>th</sup> International Symposium on Computer Architecture (ISCA '02)</i> , May 25-29, 2002, Anchorage, AK, USA: IEEE Computer Society 2002, pp. 158-168.	
C27	Joon-Seo, Yim, et al., "A C-based RTL Design Verification Methodology For Complex Microprocessor" <i>Proceedings of the Design Automation Conference</i> . Anaheim, June 9-13, 1997, New York, ACM, IS, vol. CONF. 34, 09-Jun-1997, pages 83-88.	
C28	Ju, Y-C, et al., "Incremental Circuit Simulation Using Waveform Relaxation" <i>Proceedings of the ACM/IEEE Design Automation Conference</i> . Anaheim, June 8-12, 1992, <i>Proceedings of the ACM/IEEE Design Automation Conference (DAC)</i> , Los Alamitos, IEEE Comp. Soc. Press, US, vol. CONF. 29, 08-Jun-1992, pages 8-11.	
C29	Jung, Y. et al., "simCore: an event driven simulation framework for performance evaluation of computer systems" <i>Modeling, analysis and simulation of computers and telecommunication systems</i> , 2000. <i>Proceedings. 8<sup>th</sup> International Symposium on San Francisco, CA, USA 29 Aug. - 1 Sept. 2002</i> .	
C30	Kim, M.G. et al., "Implementation of a Cycle-Based Simulator for the Design of a Processor Core," <i>Proceedings of AP-ASIC '99: The First IEEE Asia-Pacific Conference on ASICs</i> , Aug. 23-25, 1999, Seoul, South Korea: 1999 IEEE, pp. 108-111.	
C31	Kravitz, S.A. et al., "Massively parallel switch-level simulation : A feasibility study" <i>IEEE Inc.</i> New York, US, vol. 10, no. 7, 01-Jul-97, pages 871-894.	
C32	Krishnaswamy, V. et al., "Parallel Compiled Event Driven VHDL Simulation" <i>Conference Proceedings of the 1998 International Conference on Supercomputing</i> ACM New York, NY, USA, July 1997, pages 297-304.	
C33	Kudlugi, M. et al., "Static Scheduling of Multiple Asynchronous Domains for Functional Verification," <i>DAC 2001</i> , June 18-22, 2001, Las Vegas, Nevada, USA: 2001 ACM, 6 pages.	
C34	Liu, J. et al., "Software Timing Analysis Using HW/SW Cosimulation and Instruction Set Simulator," <i>Proceedings of the Sixth International Workshop on Hardware/Software Codesign (CODES/CASHE '98)</i> , March 15-18, 1998, Seattle, Washington, USA: 1998 IEEE, pp. 65-69.	
C35	Maurer, P.M., "Scheduling Blocks for Heirarchical Compiled Simulation," Technical Report DA-23, 1991, VCAPP Laboratory, University of South Florida, <a href="ftp://pangolin.csee.usf.edu/pub/facul.ty/maurer/tech-reports/da23_91.pdf">ftp://pangolin.csee.usf.edu/pub/facul.ty/maurer/tech-reports/da23_91.pdf</a> , 23 pages.	
C36	McCammon, R. et al., "Cycle-accurate model speeds design," <i>EE Times</i> , <a href="http://www.eetimes.com/story/OEG19990615S0021">http://www.eetimes.com/story/OEG19990615S0021</a> ; November 13, 2002, 6 pages.	
EXAMINER		DATE CONSIDERED



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		FILING DATE: 8-Apr-2004      GROUP: 2123
OTHER ART, JOURNAL ARTICLES, ETC.		
C37	Palnitkar, S. et al., Sun Microsystems, Inc., "Cycle Simulation Techniques," <i>Proceedings of the 1995 IEEE International Verilog HDL Conference</i> , March 27-29, 1995, Santa Cruz, CA, USA: IEEE Computer Society Press, 1995, pp. 2-8.	
C38	Paul, J.M. et al., "Frequency Interleaving as a Codesign Scheduling Paradigm," <i>Proceedings of the Eighth International Workshop on Hardware/Software Codesign</i> , May 3-5, 2000, San Diego, CA, USA: CODES 2000, ACM 2000, pp. 131-135.	
C39	Schulz, S.E., "Timing analysis tools in the critical path have a crucial impact on the success of a design," <i>EEdesign</i> , <a href="http://www.eedesign.com/editorial/2000/focusreport0008.html">http:// www.eedesign.com/editorial/2000/focusreport0008.html</a> ; November 13, 2002, 6 pages.	
C40	Stoye, W. et al., "Using Tenison VTOC™ for Large SoC Concurrent Engineering: A Real World Case Study," <i>GlobespanVirata</i> , TenisonEDA, <a href="http://www.tenison.com">www.tenison.com</a> ; pp. 1-13.	
C41	Sun Young Hwang, "Incremental algorithms for digital simulation" <i>Integration, The VLSI Journal</i> , North-Holland Publishing Company. Amsterdam, NL, vol. 7, no. 1, 01-Apr-1989, pages 21-34.	
C42	Tabbara, B. et al., "Fast Hardware-Software Co-Simulation Using VHDL Models," <i>Proceedings; Design, Automation and Test in Europe. Conference and Exhibition</i> , 1999, Munich, Germany, March 9-12, 1999. IEEE Computer Society 1999, pp. 309-316.	
C43	TenisonEDA, "Engineering Management in the SOC Era," <a href="http://www.tenison.com">www.tenison.com</a> , 1 page.	
C44	TenisonEDA, "Hardware/Software Co-Design in the SOC Era," <a href="http://www.tenison.com">www.tenison.com</a> ; pp. 1-7.	
C45	TenisonEDA, "Introducing VTOC™: Bridging the SOC Co-Development Gap," <i>Tenison EDA World Tour</i> , September 2002, <a href="http://www.tenison.com">www.tenison.com</a> , 14 pages.	
C46	TenisonEDA, "VTOC 1.0 User Guide," <a href="http://www.tenison.com">www.tenison.com</a> ; pp. 1-51.	
C47	Tension Technology, "A Verilog to C Compiler," <i>Submitted to IEEE Transactions on Software Engineering</i> , pp. 1-10	
C48	Tenison Technology: Hardware & Software Working Together, "New cycle-based Verilog Compiler is 50 to 100 times faster than behavioural simulation," <a href="http://www.tenisontech.com/news/nw010302.htm">www.tenisontech.com/news/nw010302.htm</a> ; March 1, 2002, 1 page.	
C49	Tensilica, "Synopsys and Tensilica Partner to Provide New Cycle-Accurate Model Generation Platform," <a href="http://www.tensilica.com/html/pr_2000_05_24.html">http://www.tensilica.com/html/pr_2000_05_24.html</a> ; November 13, 2002, 3 pages.	
C50	Ye, W. et al., "The Design and Use of SimplePower: A Cycle-Accurate Energy Estimation Tool," <i>Proceedings of the 37<sup>th</sup> Design Automation Conference</i> , Los Angeles, CA, USA: DAC 2000, 2000 ACM, pp. 340-345.	
EXAMINER		DATE CONSIDERED